**IN THE CLAIMS**

Please amend the Claims as follows:

1 (Amended). A semiconductor stacking structure comprising:

a first semiconductor device; and

a flexible substrate having metal layers for electrical connections coupled to a bottom surface of the first semiconductor device via the metal layers wherein the flexible substrate is folded over on at least two sides so as to not overlap and to form flap portions which are coupled to an upper surface of the first semiconductor device and wherein the flap portions cover[s] only a [portion] section of the upper surface of the first semiconductor device which is smaller than the upper surface of the first semiconductor device, the flexible substrate used for stacking additional semiconductor devices on the first semiconductor device.

2 (No Change). A semiconductor stacking structure in accordance with Claim 1 further comprising an adhesive layer which is placed on the flap portions of the flexible substrate and which couples the flap portions to the first semiconductor device.

3 (No Change). A semiconductor package in accordance with Claim 1 further comprising an adhesive layer which is placed on the upper surface of the first semiconductor device and which couples the flap portions to the first semiconductor device.

4 (No Change). A semiconductor stacking structure in accordance with Claim 1 further comprising a second semiconductor device coupled to the flap portions of the flexible substrate.

5 (No Change). A semiconductor stacking structure in accordance with Claim 4 wherein the second semiconductor device is coupled to the flap portions of the flexible substrate after the flap portions are folded over and coupled to the first semiconductor device.

6 (No Change). A semiconductor stacking structure in accordance with Claim 4 wherein the second semiconductor device is coupled to the flap portions of the flexible substrate before the flap portions are folded over and coupled to the first semiconductor device.

7 (No Change). A semiconductor stacking structure package in accordance with Claim 1 wherein the semiconductor stacking structure is a LGA (Land Grid Array) device.

8 (No Change). A semiconductor stacking structure in accordance with Claim 1 wherein the semiconductor stacking structure is a BGA (Ball Grid Array) device.

9 (No Change). A semiconductor stacking structure in accordance with Claim 1 wherein the semiconductor stacking structure is a lead type of device.

10 (No Change). A semiconductor stacking structure in accordance with Claim 1 wherein the flexible substrate is folded over on four sides to form flap portions which are coupled to the upper surface of the first semiconductor device and covers only a portion of the upper surface of the first semiconductor device.

11 (Amended). A semiconductor stacking structure comprising:

a first semiconductor device; and

means <u>having metal layers for electrical connections</u> coupled to a bottom surface of the first semiconductor device <u>via the metal layers</u> for forming the semiconductor stacking structure wherein the means is folded over on at least two sides <u>so as to not overlap</u> and coupled to an upper surface of the first semiconductor device and covers only a portion of the upper surface of the first semiconductor device <u>which is smaller than the upper surface of the first semiconductor device, the flexible substrate used for stacking additional semiconductor devices on the first semiconductor device</u>.

12 (No Change). A semiconductor stacking structure in accordance with Claim 11 further comprising an adhesive layer placed on the means for coupling the means to the upper surface of the first semiconductor device.

13 (Examiner Withdrawals From Consideration).

14 (Examiner Withdrawals From Consideration).

15 (Examiner Withdrawals From Consideration).

16 (Examiner Withdrawals From Consideration).

17 (Examiner Withdrawals From Consideration).

18 (Examiner Withdrawals From Consideration).

19 (Examiner Withdrawals From Consideration).

20 (Examiner Withdrawals From Consideration).

21 (Amended). A semiconductor stacking structure comprising:

a first semiconductor device; and

means having metal layers for electrical connections coupled to a bottom surface of the first semiconductor device via the metal layers for forming the semiconductor stacking structure wherein the means is folded over on at least two sides so as to not overlap to form flap portions which are coupled to an upper surface of the first semiconductor device and covers only a portion of the upper surface of the first semiconductor device which is smaller than the upper surface of the first semiconductor device, the flap portions increasing connect density of the semiconductor stacking structure and used for stacking additional semiconductor devices on the first semiconductor device.

22 (No Change). A semiconductor stacking structure in accordance with Claim 21 further comprising means placed on the flap portions of the flexible substrate for coupling the flap portions to the first semiconductor device.

23 (No Change). A semiconductor package in accordance with Claim 21 further comprising means placed on the upper surface of the first semiconductor device for coupling the flap portions to the first semiconductor device.

24 (No Change). A semiconductor stacking structure in accordance with Claim 21 further comprising a second semiconductor device coupled to the flap portions of the means.

25 (No Change). A semiconductor stacking structure in accordance with Claim 24 wherein the second semiconductor device is coupled to the flap portions of the means after the flap portions are folded over and coupled to the first semiconductor device.

26 (No Change). A semiconductor stacking structure in accordance with Claim 24 wherein the second semiconductor device is coupled to the flap portions of the means before the flap portions are folded over and coupled to the first semiconductor device.

27 (No Change). A semiconductor stacking structure package in accordance with Claim 21 wherein the semiconductor stacking structure is a LGA (Land Grid Array) device.

28 (No Change). A semiconductor stacking structure in accordance with Claim 21 wherein the semiconductor stacking structure is a BGA (Ball Grid Array) device.

## CLEAN VERSION OF THE CLAIMS

1. A semiconductor stacking structure comprising:

a first semiconductor device; and

a flexible substrate having metal layers for electrical connections coupled to a bottom surface of the first semiconductor device via the metal layers wherein the flexible substrate is folded over on at least two sides so as to not overlap and to form flap portions which are coupled to an upper surface of the first semiconductor device and wherein the flap portions cover only a section of the upper surface of the first semiconductor device which is smaller than the upper surface of the first semiconductor device, the flexible substrate used for stacking additional semiconductor devices on the first semiconductor device.

2. A semiconductor stacking structure in accordance with Claim 1 further comprising an adhesive layer which is placed on the flap portions of the flexible substrate and which couples the flap portions to the first semiconductor device.

3. A semiconductor package in accordance with Claim 1 further comprising an adhesive layer which is placed on the upper surface of the first semiconductor device and which couples the flap portions to the first semiconductor device.

4. A semiconductor stacking structure in accordance with Claim 1 further comprising a second semiconductor device coupled to the flap portions of the flexible substrate.

5. A semiconductor stacking structure in accordance with Claim 4 wherein the second semiconductor device is coupled to the flap portions of the flexible substrate after the flap portions are folded over and coupled to the first semiconductor device.

6. A semiconductor stacking structure in accordance with Claim 4 wherein the second semiconductor device is coupled to the flap portions of the flexible substrate before the flap portions are folded over and coupled to the first semiconductor device.

7. A semiconductor stacking structure package in accordance with Claim 1 wherein the semiconductor stacking structure is a LGA (Land Grid Array) device.

8. A semiconductor stacking structure in accordance with Claim 1 wherein the semiconductor stacking structure is a BGA (Ball Grid Array) device.

9. A semiconductor stacking structure in accordance with Claim 1 wherein the semiconductor stacking structure is a lead type of device.

10. A semiconductor stacking structure in accordance with Claim 1 wherein the flexible substrate is folded over on four sides to form flap portions which are coupled to the upper surface of the first semiconductor device and covers only a portion of the upper surface of the first semiconductor device.

11. A semiconductor stacking structure comprising:

a first semiconductor device; and

means having metal layers for electrical connections coupled to a bottom surface of the first semiconductor device via the metal layers for forming the semiconductor stacking structure wherein the means is folded over on at least two sides so as to not overlap and coupled to an upper surface of the first semiconductor device and covers only a portion of the upper surface of the first semiconductor device which is smaller than the upper surface of the first semiconductor device, the flexible substrate used for stacking additional semiconductor devices on the first semiconductor device.

12. A semiconductor stacking structure in accordance with Claim 11 further comprising an adhesive layer placed on the means for coupling the means to the upper surface of the first semiconductor device.

13 (Examiner Withdrawals From Consideration).

14 (Examiner Withdrawals From Consideration).

15 (Examiner Withdrawals From Consideration).

16 (Examiner Withdrawals From Consideration).

17 (Examiner Withdrawals From Consideration).

18 (Examiner Withdrawals From Consideration).

19 (Examiner Withdrawals From Consideration).

20 (Examiner Withdrawals From Consideration).

21. A semiconductor stacking structure comprising:

a first semiconductor device; and

means having metal layers for electrical connections coupled to a bottom surface of the first semiconductor device via the metal layers for forming the semiconductor stacking structure wherein the means is folded over on at least two sides so as to not overlap to form flap portions which are coupled to an upper surface of the first semiconductor device and covers only a portion of the upper surface of the first semiconductor device which is smaller than the upper surface of the first semiconductor device, the flap portions increasing connect density of the semiconductor stacking structure and used for stacking additional semiconductor devices on the first semiconductor device.

22. A semiconductor stacking structure in accordance with Claim 21 further comprising means placed on the flap portions of the flexible substrate for coupling the flap portions to the first semiconductor device.

23. A semiconductor package in accordance with Claim 21 further comprising means placed on the upper surface of the first semiconductor device for coupling the flap portions to the first semiconductor device.

24. A semiconductor stacking structure in accordance with Claim 21 further comprising a second semiconductor device coupled to the flap portions of the means.

25. A semiconductor stacking structure in accordance with Claim 24 wherein the second semiconductor device is coupled to the flap portions of the means after the flap portions are folded over and coupled to the first semiconductor device.

26. A semiconductor stacking structure in accordance with Claim 24 wherein the second semiconductor device is coupled to the flap portions of the means before the flap portions are folded over and coupled to the first semiconductor device.

27. A semiconductor stacking structure package in accordance with Claim 21 wherein the semiconductor stacking structure is a LGA (Land Grid Array) device.

28. A semiconductor stacking structure in accordance with Claim 21 wherein the semiconductor stacking structure is a BGA (Ball Grid Array) device.